

EAST - [10786798b.wsp:1]

File View Edit Tools Window Help

Drafts
Pending
Active
L1: (260) split near gate and flash near memory and (thickness with (gate near insulat\$3 gate nea...
L2: (76) split near gate and flash near memory and (thickness with ((gate near insulat\$3 gate nea...
L3: (61) split near gate and flash near memory and PECVD
Failed
split near gate and flash near memory and (thickness with ((gate near insulat\$3 gate near dielect...
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DBs US-PGPUB: USPAT: USOCR Plurals
Default operator: OR Highlight all hit terms initially

split near gate and flash near memory and (thickness with ((gate near insulat\$3 gate near dielectric) and angstroms))

BRS form IS&R form Image Text HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
47	<input type="checkbox"/>	<input type="checkbox"/>	US 6706602 B2	20040316	8	Manufacturing method of flash memory	438/267	257/315; . 438/257
48	<input type="checkbox"/>	<input type="checkbox"/>	US 6704222 B2	20040309	39	Multi-state operation of dual floating gate array	365/185.03	365/185.11; 365/185.28
49	<input type="checkbox"/>	<input type="checkbox"/>	US 6690058 B2	20040210	23	Self-aligned multi-bit flash memory cell and its contactless flash memory array	257/316	257/390; 257/401; 257/E21.682.
50	<input type="checkbox"/>	<input type="checkbox"/>	US 6664587 B2	20031216	40	EEPROM cell array structure with specific floating gate shape	257/315	257/317
51	<input type="checkbox"/>	<input type="checkbox"/>	US 6642116 B2	20031104	13	Method for fabricating a split gate flash memory cell	438/286	257/E21.209; 257/E29.129; 438/257.
52	<input type="checkbox"/>	<input type="checkbox"/>	US 6635533 B1	20031021	9	Method of fabricating flash memory	438/259	438/264; 438/266; 438/267.
53	<input type="checkbox"/>	<input type="checkbox"/>	US 6620689 B2	20030916	13	Method of fabricating a flash memory cell using angled implant	438/266	257/E21.209; 257/E29.129; 438/302.
54	<input type="checkbox"/>	<input type="checkbox"/>	US 6605840 B1	20030812	19	Scalable multi-bit flash memory cell and its memory array	257/315	257/316; 257/321; 257/322.
55	<input type="checkbox"/>	<input type="checkbox"/>	US 6593187 B1	20030715	20	Method to fabricate a square poly spacer in flash	438/257	257/296; 257/300; 257/301.
56	<input type="checkbox"/>	<input type="checkbox"/>	US 6579761 B1	20030617	12	Method to improve the coupling ratio of top gate to floating gate in flash	438/257	438/266; 438/296
57	<input type="checkbox"/>	<input type="checkbox"/>	US 6570213 B1	20030527	22	Self-aligned split-gate flash memory cell and its contactless NOR-type memory array	257/315	257/314; 257/321; 257/E21.682.

Hits Details HTML

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